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Transfer Line Station with RF Tag Reader

(By Kerry L. Schrank, Senior Application Specialist)

This application note describes station number nine of a thirty-eight station transfer line operation and highlights interfacing to an RF/ID tag reader. The tag-reader chosen for this application uses a PC ISA bus controller card. No special driver for the tag reader controller card was required. Instead, this application was developed using the **Think & Do Software** generic dual port RAM driver.

The diagram below pictorially describes the components of the application, which include a PC with NT, an Escort Memory Systems HS900 PC-Bus controller, an HS500 antenna and an HS200R tag. While any I/O network could be used for discrete device control, Honeywell's Smart Distributed Control System was chosen for this application.

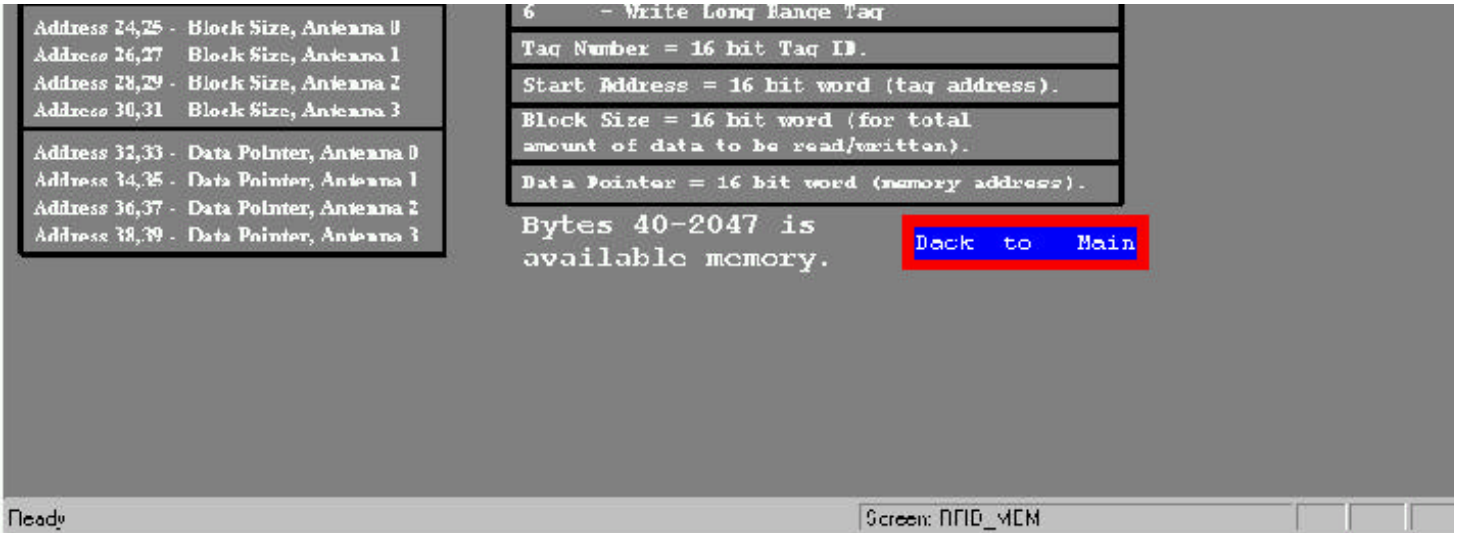
Think & Do software makes it easy for users to interface to PC cards for devices and I/O where a specific driver is not supported by **Think & Do**. **Think & Do's** generic dual port ram driver gives users a graphical interface to a memory mapped or IO port mapped ISA bus card using flowcharts instead of using other programming tools such as Visual Basic or Visual C++. The user only has to know the start address of the memory space occupied by the card (the board address is typically jumper selectable) and the size of the dual port memory. (To maintain maximum predictability and performance the generic dual port ram driver is part of the **Think & Do** I/O scan cycle which guarantees it adequate CPU resources.)

Defining the Memory Map

Once the definition of memory is understood, the user configures the generic dual port ram driver.

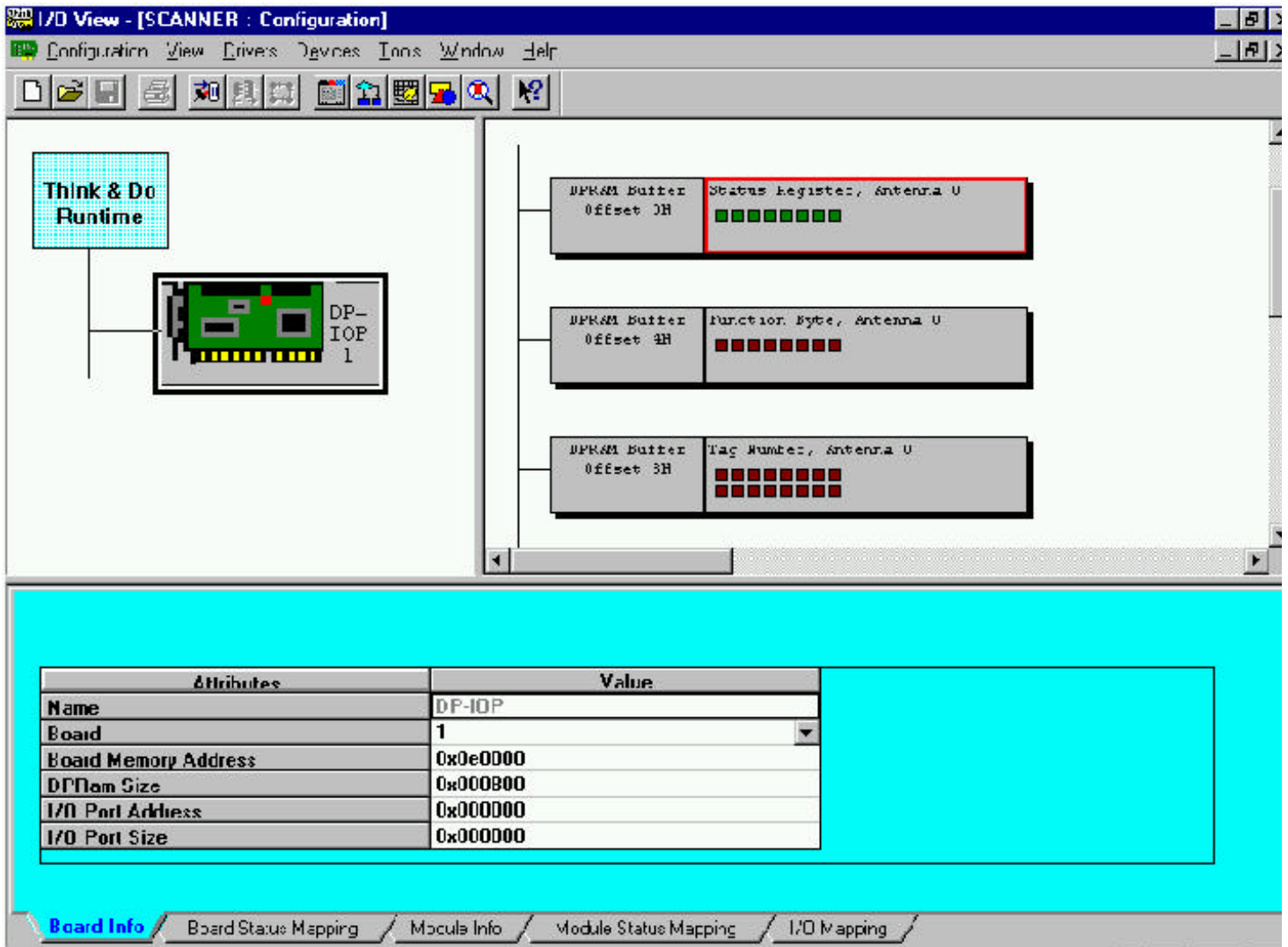
The following screen defines the memory map of the RF/ID scanner card. The first 40 bytes of memory (of a 2K memory map) shown in the first column comprise the Status, Function, Tag Number, Start Address, Block Size and Data Pointer bytes for configuring the four antennas supported by the PC controller card. The second column gives the description of each byte or word for interfacing to the controller card. Note that bytes 40 through 2047 are general memory usage for storing the alphanumeric data for the tags.

RFID Memory Map 2k DPRAM	Description of Bytes
Address 0 - Status Byte, Antenna 0	Status byte: Written by the Controller Card and read by the Host. 16 - Battery reset in progress 8 - Read in Progress 4 - Write in Progress 2 - Read Complete 1 - Write Complete 0 - Device Ready
Address 1 - Status Byte, Antenna 1	
Address 2 - Status Byte, Antenna 2	
Address 3 - Status Byte, Antenna 3	
Address 4 - Function Byte, Antenna 0	Function byte: Written by the Host and read by the Controller. 0 - Do nothing 1 - Read 2 - Write 3 - Battery Timer Reset 4 - Inquire Version 5 - Read Long Range Tag
Address 5 - Function Byte, Antenna 1	
Address 6 - Function Byte, Antenna 2	
Address 7 - Function Byte, Antenna 3	
Address 8,9 - Tag Number, Antenna 0	
Address 10,11 - Tag Number, Antenna 1	
Address 12,13 - Tag Number, Antenna 2	
Address 14,15 - Tag Number, Antenna 3	
Address 16,17 - Start Address, Antenna 0	
Address 18,19 - Start Address, Antenna 1	
Address 20,21 - Start Address, Antenna 2	
Address 22,23 - Start Address, Antenna 3	



IOView Tool (adding the driver and devices)

Below is picture of **Think & Do's** IOView tool. This is where the user adds the generic dual port ram driver, enters the starting address of memory (in this application 0x0E000) and enters the size of memory (in this case 0x00800). One then simply adds devices, which are basically, pointers into the area of memory that the user defined.



For help, press F1

These devices can be 1, 2, 4, 8, 16, 32 or 64 bits and can be read only, write only or read and write. Each device is given an offset from the beginning of the dual ported ram that the user must know or calculate. Then each bit of the device is mapped to the tag name database in the same way one maps physical IO. In this application, the Status register for antenna zero is an eight bit read only device and has an offset of zero (because it is the first address in the dual ported memory). The Function Byte (or control register) is an eight-bit write only device with an offset of four (hex). The rest of the dual ported memory is mapped in this fashion. The user can automatically scan the defined memory area and view the data in real time - all with no programming! In addition, I/O View enables the user to assign an appropriate name to the device which can then be used to reference the defined portion of memory.

Once the data items from the database have been mapped, flow charts can be written to control reading/writing data from/to the dual port ram. One key feature of the generic dual port RAM driver is that it gives the user full control over the timing of writes to memory. The user can write each bit or byte individually, or can easily specify a set of changes to be written concurrently. All of this is done in the same easy to read flowcharts that are used for control logic. There is no new programming language to learn and no special scripting mechanism to figure out.

Think & Do Software gives the user two ways to enable writing to memory. The first is to simply set the WriteEveryScan bit and the second is to enable the TriggerWrite bit. These bits are enabled in a flow chart using a control block. Don't forget to include enabling these bits or you will never write data to memory!

Think & Do Runtime

DP-IOP 1

DPRAM Buffer Offset 0H Status Register, Antenna 0

DPRAM Buffer Offset 4H Function Byte, Antenna 0

DPRAM Buffer Offset 3H Tag Number, Antenna 0

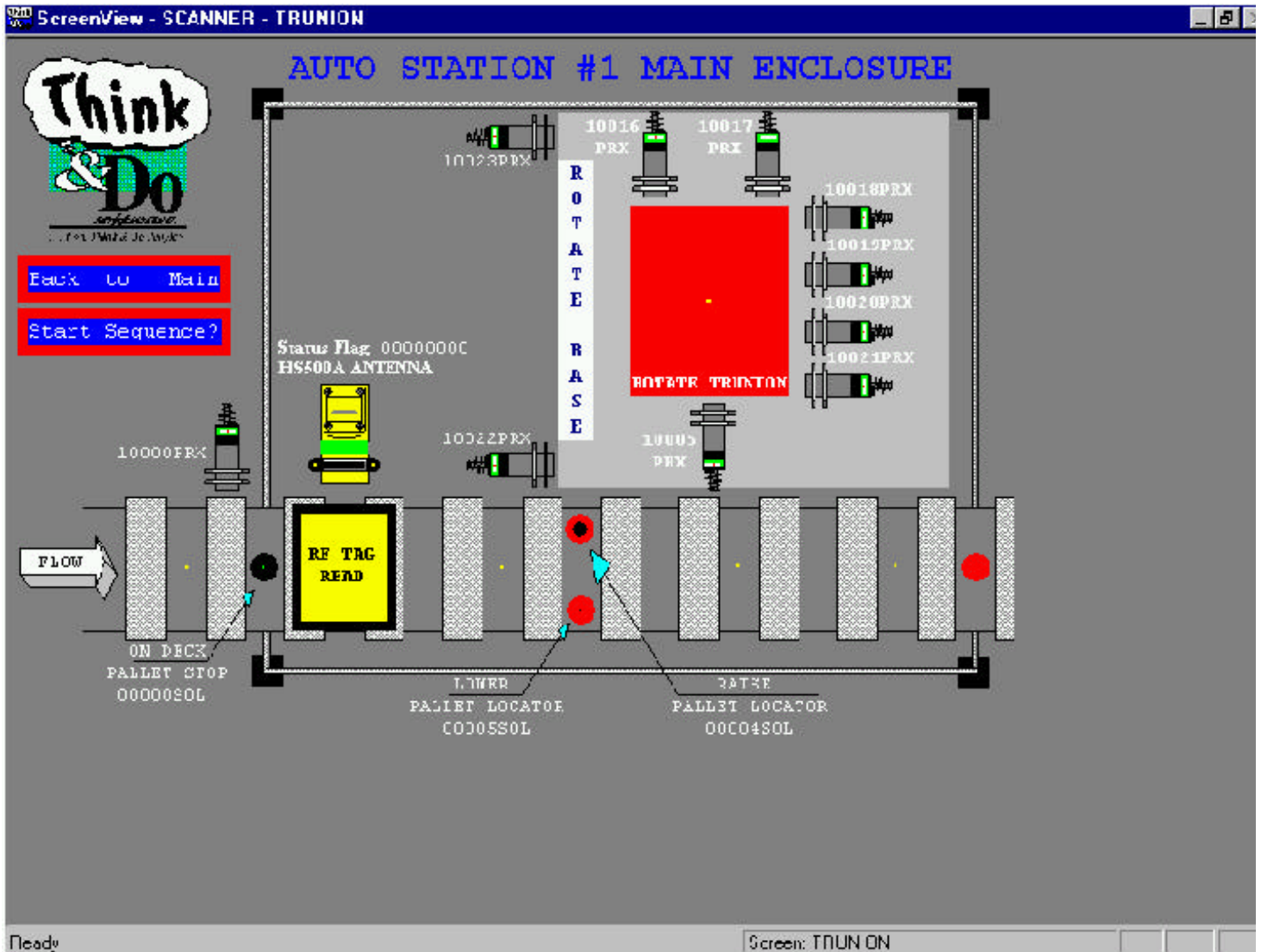
Status Item	Description	Data Type	Logical ID	Tagname	Value
1	DP-IOP_Bd1_Nd3_Offset008_ErrorExists	Input			0
2	DP-IOP_Bd1_Nd3_Offset008_Invalid Offset	Input			0
3	DP-IOP_Bd1_Nd3_Offset008_WriteEveryScan	Output			0
4	DP-IOP_Bd1_Nd3_Offset008_TriggerWrite	Output	0 26	Tag Number Trigger	0

Board Info / Board Status Mapping / Module Info / **Module Status Mapping** / I/O Mapping

Now that the driver is configured, the user can develop the appropriate flow charts to read and write data from and to the dual ported memory. Of course, configuring the IO map could have been completed after the flow charts were developed. The next screen in this example shows run-time screen of the project.

Run-time Screen

The following screen depicts the flow of the transfer line. Devices enter the station and the RF tag is read in the position shown on the screen. The different sensors depict the states of the sequence of operation. The device enters the trunion, the trunion is rotated by ninety degrees and then the device exits the station.



The devices and the associated alphanumeric data may easily be tracked using strings and arrays, which are part of the **Think&Do** database.

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